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AI INTEGRATION IN ELECTRONIC CIRCUIT DESIGN FOR ENHANCED PERFORMANCE

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Abstract

The integration of machine learning (ML) into integrated circuit (IC) synthesis is revolutionizing electronic circuit design by addressing the computational inefficiencies of traditional methods. While optimization-based synthesis is effective, it often requires extensive simulations, many of which are underutilized. ML reduces these computational costs by developing predictive models that can replace traditional circuit simulators, thereby accelerating design iterations. Techniques such as artificial neural networks (ANNs) and reinforcement learning (RL) have proven particularly valuable in creating technology-independent circuit designs and enabling autonomous circuit generation, enhancing both accuracy and efficiency. By leveraging large datasets, ML can simulate complex circuits like operational amplifiers (Op-Amps) and optimize parameters with minimal additional simulations. Moreover, ML enhances fault diagnosis and post-fabrication calibration through dimensionality reduction and Bayesian model fusion, streamlining the design process and improving yield. As a result, ML-based approaches offer a significant advancement in circuit synthesis, reducing time, cost, and reliance on traditional, simulation-heavy methods, thereby paving the way for enhanced performance in electronic circuit design.

Keywords: *Machine Learning (ML)[1], Circuit Synthesis[2], Optimization3, Artificial Neural Networks (ANN)[4], Reinforcement Learning (RL)[5].*

1. Introduction

The integration of machine learning (ML) into integrated circuit (IC) synthesis is transforming electronic circuit design by addressing the inefficiencies of traditional methods. While optimization-based synthesis is effective, it often requires extensive simulations, many of which are underutilized. ML mitigates these computational demands by developing predictive models that replace traditional circuit simulators, thereby accelerating design iterations. Techniques such as artificial neural networks (ANNs) and reinforcement learning (RL) have proven particularly valuable in creating technology-independent circuit designs and enabling autonomous circuit generation, enhancing both accuracy and efficiency. By leveraging large datasets, ML can simulate complex circuits like operational amplifiers (Op-Amps) and optimize parameters with minimal additional simulations. Additionally, ML enhances fault diagnosis and post-fabrication calibration through dimensionality reduction and Bayesian model fusion, streamlining the design process and improving yield. Consequently, ML-based approaches significantly advance circuit synthesis, reducing time, cost, and reliance on traditional methods, paving the way for enhanced performance in electronic circuit design.

2. Machine Learning for IC Circuit Synthesis

ML for Optimization-based Circuit Synthesis: In traditional circuit synthesis, the process is typically automated to determine the dimensions of devices to meet specific target specifications for a given technology node. Simulation-based approaches are the most commonly used for evaluation due to their accuracy. However, SPICE-based circuit synthesis can be costly in terms of computation time, requiring tens of thousands of simulations to achieve the desired performance. To address this inefficiency, machine learning (ML)-based synthesis methods have gained popularity. ML techniques replace extensive simulations with functional models, reducing the need for numerous simulations during synthesis. Optimization-based circuit synthesis is a well-established method that uses optimization techniques to explore the design space, accelerating design time. This approach employs nature-inspired algorithms, such as evolutionary algorithms, particle swarm optimization, and reinforcement learning, to find optimal solutions. Despite its effectiveness, optimization-based methods often require extensive simulations, with many results being unused by the end of the process. Integrating ML into the conventional optimization loop offers a promising solution to reduce computational costs by reusing simulation data to develop models that can replace circuit simulators.

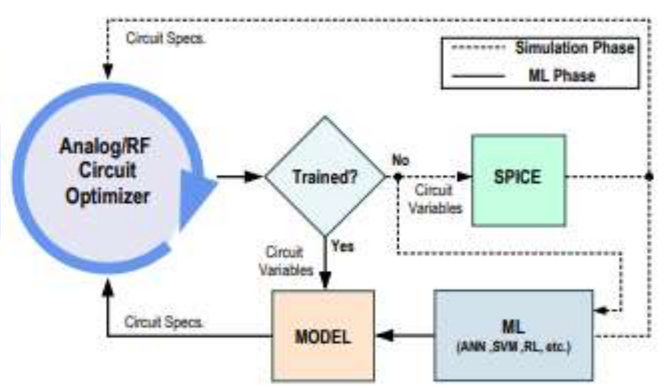

Figure 1 A general flow of the ML-based analog/RF circuit optimization

Typically, ML models emulate circuit behavior as a function of design variables. However, it is also possible to model design variables as functions of objectives. Some approaches involve using optimization tools to generate datasets for ML, applying regression models to fit high-dimensional data points. For example, using radial basis functions or posynomial-approximated signomials, and employing a committee of regressors combined with k-nearest neighbors (KNN) algorithms, can effectively fit data across large design spaces. This approach has been demonstrated in cases such as RF low noise amplifiers (LNAs), where models evolve to focus on specific regions of the design space, improving accuracy as synthesis progresses.

ML-Based Circuit Synthesis: In traditional circuit design, the process typically begins with selecting a suitable topology from various options and then sizing the circuit according to that topology. If the technology or specifications change, the circuit often needs to be redesigned, even if the topology remains the same. Generally, technology parameters and device dimensions are considered inputs for the circuit. Once a topology is accurately trained using machine learning (ML), the model can provide solutions for different technologies without requiring additional simulations. For instance, one approach uses an artificial neural network (ANN) for technology-independent design of a current steering PMOS-only digital-to-analog converter (DAC). The goal is to derive design parameters for new technologies without running additional circuit simulations. This involves creating a large database of current steering DAC designs through numerous simulations across different technologies. Key specifications such as static specification parameters (SSP), differential nonlinearity (DNL) error, integral nonlinearity (INL) error, monotonicity, and gain error are used as inputs, with transistor dimensions as outputs. The General Regression Neural Network (GRNN) was employed, demonstrating that the ANN-based approach could design circuits for new technologies and improve specifications such as monotonicity and reduction in errors.

Similarly, ANN-assisted technology-independent sizing for building blocks like basic current mirrors and differential amplifiers used in analog integrated circuits has been explored. The models were trained with data from various technologies and tested on a new technology to verify the approach's independence from specific technologies. GRNN and Multi-Layer Perceptron (MLP) with the Rprop algorithm were used. The models accurately provided transistor sizes with high accuracy, maintaining a tolerance for circuit performance. To address the challenge of generating large training datasets, a method for a current-to-voltage converter circuit involves two levels of data generation for training and testing the ANN, with an MLP model implemented to map inputs (current and gate-to-source voltage) to outputs (channel length and width). Simulations were conducted by varying transistor dimensions and input currents, achieving high accuracy in estimating the output voltage.

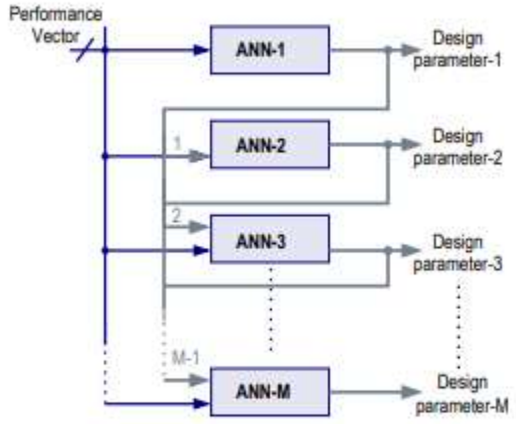

Figure 2 The block diagram of the ANN array methodology

More complex circuits, such as a three-stage operational amplifier (Op-Amp), have been analyzed. In this case, samples were generated through SPICE simulations, with a portion used for training and the rest for testing. The ANN model, consisting of multiple layers, achieved low error after several training epochs. The results were validated against simulations, meeting all targeted specifications and demonstrating high figures of merit for both large and small signal operations. Additionally, a deep learning-based methodology for Op-Amp sizing predicts circuit element values from performance specifications through regression analysis. This approach involves generating and normalizing a large dataset of specifications and transistor widths. The learning phase includes data classification, collection, and normalization. An initial dataset of elements was simulated, with solutions evaluated against a predefined figure of merit. The final model predicted circuit performances with high accuracy.

3. Reinforcement Learning in Circuit Synthesis

Reinforcement Learning (RL) addresses complex problems through an iterative trial-and-error approach, akin to human learning. An RL agent interacts with an environment, where it learns from rewards based on actions taken, as shown in Figure 3. The agent transforms the current state (St) and reward (Rt) into an action, while the environment updates the state to (St+1) and assigns a new reward (Rt+1) based on the action taken. This loop generates a sequence of states, actions, and rewards. Training large-scale datasets for circuit design is challenging due to slow simulations and proprietary designs. To overcome this, an RL-based method was proposed to generate circuits autonomously. Initially, the RL agent learns to meet constraints and then optimizes targets. Compared to grid search methods, this approach achieves 250× higher sample efficiency with similar performance. The RL agent, trained without prior knowledge of analog design, learns from data to search for optimal parameters and has been successfully applied to Op-Amp circuits.

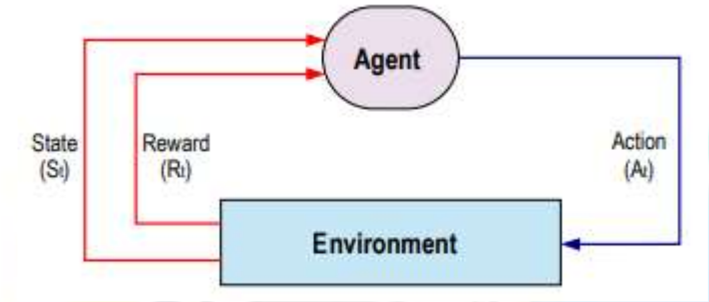

Figure 3 The agent-environment interaction in reinforcement learning loop

A deep reinforcement learning framework for analog circuit sizing uses a Policy Gradient Neural Network (PGNN). The PGNN predicts changes in circuit parameters, defining actions as adjustments to these parameters. Actions that do not meet design constraints are eliminated before simulation, reducing execution time. The system uses a symbolic filter for initial evaluations, followed by SPICE simulations. The method has been demonstrated on a folded cascode amplifier, optimizing for specifications like gain, bandwidth, and margins, achieving satisfactory results. Another approach focuses on post-layout circuit parameters using deep RL, which involves two steps: training and deployment. During training, performance trajectories are obtained through SPICE simulations, and the RL agent updates its neural network based on observed and targeted specifications. The agent learns to adjust parameters to meet design constraints and objectives, terminating training when specifications are met. In deployment, the trained agent generates trajectories for new specifications and is integrated with a layout generator tool for post-layout simulations. This approach has shown to be 40× more sample efficient than traditional genetic algorithms and 9.6× more efficient in post-layout simulations, demonstrating effective learning transfer from schematic to layout.

4. Pre-Processing with Dimensionality Reduction

In advanced fault diagnosis systems, data processing pipelines are crucial for handling complex feature spaces. The process typically begins with collecting and transforming raw data. Techniques like wavelet transformations compress this data into meaningful coefficients. Following transformation, dimensionality reduction is applied using methods such as Principal Component Analysis (PCA) or Linear Discriminant Analysis (LDA). These methods simplify the data while retaining essential features, making it more manageable for classification. A fault dictionary catalogs characteristics of different circuit faults, which helps in feature extraction. PCA reduces the dimensionality of fault data, and the relevant features are selected based on measures like distance separation. Artificial Neural Networks (ANNs) are then trained in this reduced feature space to classify circuits as faulty or fault-free. This approach has demonstrated high accuracy in various analog circuit applications. Other techniques, such as Haar wavelet transforms and modified kernel PCA, further enhance feature extraction and separation. Sinusoidal excitation and oblique Fisher decision trees are also used to improve classification accuracy.

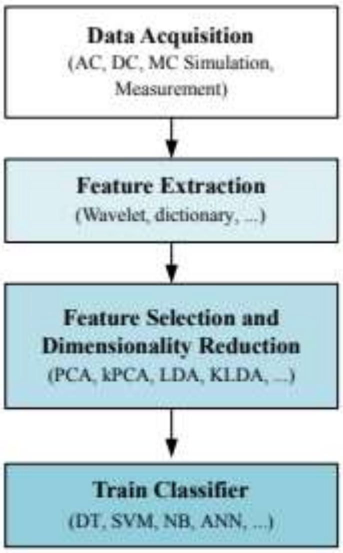

Figure 4 Common pipeline used on recent fault diagnosis systems

Some methods involve time-frequency matrices and advanced feature selection, though these can be computationally demanding. Overall, dimensionality reduction and pre-processing are critical for effective fault diagnosis in complex electronic circuits.

5. Shortening the ML Pipeline with DBNs

Traditional fault diagnosis methods often involve compressing high-dimensional system outputs into lower-dimensional features for fault isolation. In contrast, recent approaches leverage Deep Learning (DL) to analyze raw output signals directly. For instance, Gaussian–Bernoulli Deep Belief Networks (GB-DBNs) are used to capture hierarchical representations of these signals without needing access to internal nodes of analog ICs, overcoming limitations of equation-based methods. The GB-DBN classifier employs a semi-supervised learning framework, consisting of two phases: unsupervised pre-training and supervised fine-tuning. The pre-training phase involves training each layer of a stacked Restricted Boltzmann Machine (RBM) independently, while the fine-tuning phase adjusts all RBM layers based on classification errors. This method enhances the separation between different fault classes and reduces within-class variation, resulting in improved diagnostic performance with fewer features.

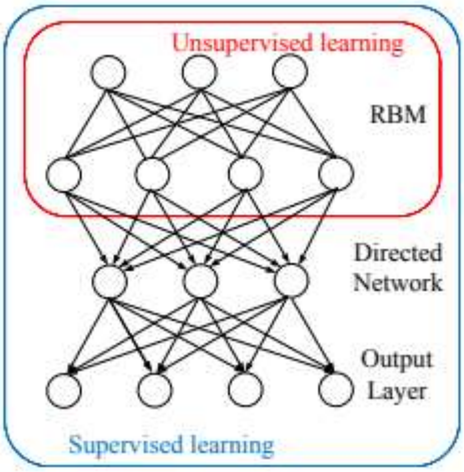

Fig. 5 DBN structure, showing hidden RBM that are trained in unsupervised learning

Another approach integrates Monte Carlo sampling with DBNs for adaptive feature extraction and dimensionality reduction. The process involves identifying potential fault modes, obtaining raw time-series signals through simulation, building a dataset, and training the DBN with unsupervised and supervised stages. This method has shown higher classification accuracy and reduced dependency on extensive data by using raw time-series signals, effectively identifying faults reflected in specific time series segments.

6. Post-Fabrication Automatic Calibration

Beyond fault identification, Machine Learning (ML) is increasingly used for specification testing and calibration of analog circuits to address process variations. These techniques enhance device quality, reduce testing costs, and increase production yield. For example, one approach uses ML to identify a minimal subset of tests for performance evaluation. Circuits failing any test in this subset are discarded, while those passing are classified using KNN and ontogenic neural networks. The subset of tests is optimized using NSGA-II to balance test cost and accuracy. Applied to an RF device, this method detected most failing circuits without specific RF testing equipment, and with some RF testing, it detected all failures at under 10% of the typical cost.

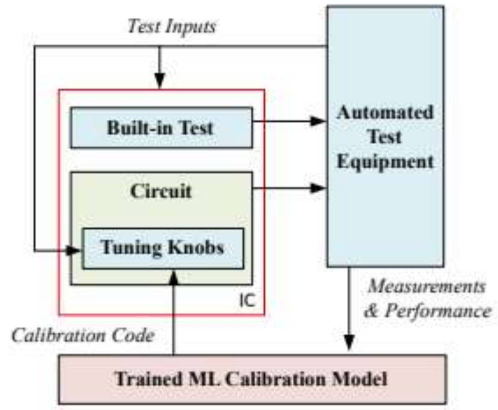

Figure 6 One-shot calibrations of fabricated circuits

Another approach involves a One-Shot calibration mechanism, depicted in Fig. 6. This method uses an Artificial Neural Network (ANN) to predict circuit performance based on test measurements and tuning knob settings. A dataset with 67 fixed knob settings per circuit is used to train the ANN. Once trained, the system measures the circuit, and if performance is off-spec, the trained model is used to find optimal knob settings. Applied to an RF power amplifier, this method successfully recovered 96% of devices failing specifications.

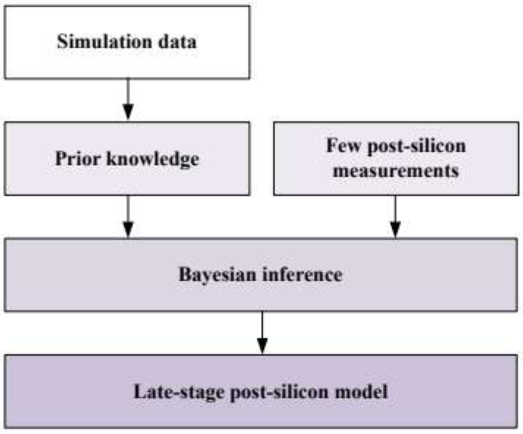

Figure 7 BMF for post-layout modeling

However, creating training data from limited silicon measurements poses challenges, as accurate modeling of parasitics and losses is complex. To address this, Bayesian model fusion, shown in Fig. 7, combines simulation-based data with actual measurements, reducing the need for extensive post-fabrication testing.

7. Conclusion

Machine learning (ML) is transforming IC circuit synthesis by addressing the computational inefficiencies of traditional methods. Optimization-based circuit synthesis, though effective, often demands extensive simulations, many of which remain unused. Integrating ML into this process reduces computational costs by developing models that replace circuit simulators, enabling faster design iterations. ML techniques, such as artificial neural networks (ANNs) and reinforcement learning (RL), are particularly effective in technology-independent circuit design and autonomous circuit generation, improving both accuracy and efficiency. These methods leverage large datasets, simulate complex circuits like Op-Amps, and optimize parameters with minimal additional simulations. Additionally, ML enhances fault diagnosis and post-fabrication calibration, using techniques like dimensionality reduction and Bayesian model fusion to streamline the design pipeline and improve yield. Overall, ML-based approaches offer a promising avenue for advancing circuit synthesis, reducing time, cost, and reliance on traditional simulation-heavy methods.

8. References

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